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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,587	04/15/2004	Arthur E. Colvin JR.	2232-171	6642
6449 7590 05/19/2008 ROTHWELL, FIGG, ERNST & MANBECK, P.C. 1425 K STREET, N.W. SUITE 800 WASHINGTON, DC 20005				
EXAMINER TANINGCO, MARCUS H				
ART UNIT 2884		PAPER NUMBER		
NOTIFICATION DATE 05/19/2008		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO-PAT-Email@rfem.com

Office Action Summary

Application No.

10/824,587

Applicant(s)

COLVIN ET AL.

Examiner

MARCUS H. TANINGCO

Art Unit

2884

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/ICE)
- Paper No(s)/Mail Date 7/12/04, 7/5/05, 11/21/06, 4/4/07, 11/5/07
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date: ____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colvin (US 2002/0026108) in view of Scarantino et al. (*Scarantino*, US 6,402,689).

With regards to claims 1 and 12, Colvin discloses a printed circuit device disposed in a sensor (Fig. 1) comprising: a substrate (70) having top and bottom surfaces, first and second side surfaces between said top and bottom surfaces along a major dimension thereof, and first and second end surfaces between said top and bottom surfaces along a minor dimension thereof; at least one circuit component (18) mounted to a main surface of said substrate; inductor coils (40, 42); and a conductor (42) formed on said substrate. Colvin fails to teach a ferrite substrate and

said conductor extends over one of said main surfaces and side surface in a coil pattern.

Scarantino discloses an implantable sensor comprising: a substrate (125P) and a conductor (58) formed on said substrate and extending over one of said main surfaces and side surfaces in a coil pattern (Figs. 7-8B). With regards to the substrate material, Scarantino teaches that the signal transmitted by the conductor is proportional to the area of the coil. Scarantino further teaches that the coil can be integrated into the circuit board itself via a ferrite substrate (column 24, lines 46-55)). As such, it would have been obvious to one with ordinary skill in the art at the time the invention was made to modify Colvin with a ferrite substrate with an integrated coil combined with a previous teaching of an external conductor in order to increase signal strength.

With regards to claims 2 and 24, Colvin fails to specifically teach said circuit component (18) comprises a lead that is routed through a via formed in said substrate. Nevertheless, those skill in the art appreciate that surface mount components can be interchanged with through hole components and is therefore viewed as a matter of routine design choice.

With regards to claim 3, Colvin discloses said circuit component (18) comprises an LED and a lead for said LED (Fig. 1).

With regards to claim 4, Colvin fails to specifically teach said lead for said LED is a drive lead. Nevertheless, those skilled in the art appreciate that, absent some degree of criticality, reconfiguration of the LED to provide a drive lead would have been a matter of routine design choice that would have been within the skill of a person of ordinary skill in the art depending on the needs of the particular application.

With regards to claims 5 and 6, Colvin fails to specifically teach how the leads of each circuit component are routed. However, those skilled in the art appreciate that, absent some

degree of criticality, routing leads to either one or a plurality of vias would have been a matter of routine design choice that would have been within the skill of a person of ordinary skill in the art depending on the needs of the particular application.

With regards to claim 7, Scarantino teaches said coil is edge-joined around said substrate (Figs. 7-8B).

With regards to claim 8, Colvin discloses said coil is used for transfer of data signals to an external device [0090].

With regards to claim 9, Colvin discloses said coil is used for inductive transfer of electric power from an external power supply (Abstract).

With regards to claim 10, Colvin discloses said printed circuit device is a component of an implantable sensor device that performs quantitative analyte measurements within a body of a living organism (Abstract).

With regards to claim 11, Colvin discloses said at least one circuit component comprises an LED (18) and wherein said printed circuit device further including at least one photodetector (20).

With regards to claims 13, 15, and 25, Colvin discloses a fluorescence sensor device (Fig. 1), comprising: a light source (18) for introducing light into a fluorescent indicator (16) that interacts with a medium; a photodetector (20) for detecting light emitted by said fluorescent indicator in response to the introduced light, and for outputting a signal proportional to the detected light, the response of the fluorescent indicator varying in accordance with the presence and quantity of an analyte in the medium; a coil for receiving electrical power from an external power supply, and for communicating said signal to an external processing device [0091];

wherein said light source, photodetector, and coil are mounted on a substrate (70); and an optical filter (34) located directly over said photodetector. Colvin fails to teach a ferrite substrate and said coil extends around opposing surfaces of a substrate. Scarantino discloses an implantable sensor comprising: a substrate (125P) and a conductor (58) formed on said substrate and extending over one of said main surfaces and side surfaces in a coil pattern (Figs. 7-8B). With regards to the substrate material, Scarantino teaches that the signal transmitted by the conductor is proportional to the area of the coil. Scarantino further teaches that the coil can be integrated into the circuit board itself via a ferrite substrate (column 24, lines 46-55)). As such, it would have been obvious to one with ordinary skill in the art at the time the invention was made to modify Colvin with a ferrite substrate with an integrated coil combined with a previous teaching of an external conductor in order to increase signal strength.

With regards to claim 14, Colvin discloses said light source and said photodetector being mounted to a first section of said substrate, and said coil being formed on a second section of said substrate (Fig. 1).

With regards to claims 16 and 23, Colvin fails to specifically teach said LED (18) comprises a lead that is routed through a via formed in said substrate. Nevertheless, those skill in the art appreciate that surface mount components can be interchanged with through hole components and is therefore viewed as a matter of routine design choice.

With regards to claim 17, Scarantino teaches said coil is edge-joined around said substrate (Figs. 7-8B).

With regards to claim 18, Colvin discloses said coil is used for transfer of data signals to an external device [0090].

With regards to claim 19, Colvin discloses said coil is used for inductive transfer of electric power from an external power supply (Abstract).

With regards to claim 20, Colvin discloses said printed circuit device is a component of an implantable sensor device that performs quantitative analyte measurements within a body of a living organism (Abstract).

With regards to claim 21, Colvin discloses said printed circuit device is a component of an implantable sensor device that performs qualitative analyte measurements within a body of a living organism (Abstract).

With regards to claim 22, Colvin discloses said light source comprises a light-emitting diode (LED) (18) said substrate further including at least one photodetector (20).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marcus H. Taningco whose telephone number is (571) 272-1848. The examiner can normally be reached on M - F 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

**/Constantine Hannaher/
Primary Examiner, Art Unit 2884**

**/Marcus H Tanningco/
Examiner, Art Unit 2884**